Breaking Symmetries in SMT Solvers

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Satisfiability Module Theories (SMT) solvers are widely used as a tool for computing combinatorial subproblems emerging from a multitude of applications, such as software verification and AI planning.

One of the recent directions in SMT solver research is based on an observation that in many applications the problem contains large amounts of symmetries. The symmetries result in the solver covering unnecessarily redundant search space, significantly increasing the solving time. The goal of this UROP project is to study how symmetries can be broken using new heuristic methods.

The work, including experimentation and implementation, will be carried out as part of the ongoing development effort of the OpenSMT solver from the Verification group at USI.

We are looking for a motivated student who wants to improve his/her knowledge on software verification and constraint-based search. This project will give the student an excellent overview of a quickly developing field while being sufficiently approachable. Prior knowledge in SMT modeling is not required, though is a plus.

The aim of this project is to integrate symmetry breaking to OpenSMT. The student will be coached while:

1. Getting familiar with the internals of SMT solvers
2. Implementing existing and developing new algorithms for symmetry detection and breaking. For this task preliminary experience with C/C++ is required.
3. Designing and running a set of experiments.